WHAT IS CLAIMED IS:

1. A data processor formed on an LSI chip comprising:

an instruction address generator generating an instruction address;

an instruction cache memory having entries each storing an instruction corresponding to the instruction address;

an instruction decoder decoding an instruction read out from said cache memory;

an operand address generator generating an operand address in response to an output signal of said instruction decoder; and

an operand cache memory having entries each storing operand data corresponding to the operand address in its entry,

wherein the data processor executes a first instruction that makes entries in both of said instruction cache memory and said operand cache memory ineffective,

wherein the first instruction is stored in a main memory with other instructions, the main memory being external to the data processor,

wherein the instruction address generator generates the instruction address as a logic address, and

wherein an address of the main memory is a physical address.

2. A data processor formed on an LSI chip according to claim 1, further comprising:

an execution unit executing an instruction based on the decoded result at said instruction decoder,

wherein said instruction decoder and said execution unit can be operated in parallel.

3. A data processor formed on an LSI chip according to claim 2, further comprising:

a ROM storing a control information corresponding to an instruction,

wherein said ROM outputs the control information corresponding to an instruction output from said instruction cache memory.

4. A data processor formed on an LSI chip according to claim 2,

wherein said execution unit has an arithmetic circuit, the arithmetic circuit computing an operand data and outputting the computed result.

5. A data processor formed on an LSI chip according to claim 2,

wherein each of entries in said instruction cache memory and said operand cache memory has a valid bit, and

wherein when said data processor executes the instruction that makes entries in both of said instruction cache memory and said operand cache memory ineffective, the valid bits of said instruction cache memory and said operand cache memory are cleared.

6. A data processor formed on an LSI chip according to claim 2,

wherein each of said instruction cache memory and said operand cache memory is an associative memory.

7. A data processor formed on an LSI chip according to claim 1,

wherein each of said instruction cache memory and said operand cache memory is an associative memory.

8. A data processor formed on an LSI chip according to claim 1,

wherein each of entries in said instruction cache memory and said operand cache memory has a valid bit, and

wherein when said data processor executes the instruction that makes entries in both of said instruction cache memory and said operand cache memory ineffective, the valid bits of said instruction cache memory and said operand cache memory are cleared.

9. A data processor formed on an LSI chip according to claim 1, further comprising:

an address transformation circuit transforming the logical address generated by said address generator to the physical address,

wherein the address transformation circuit is connected to the output part inside of the LSI chip.

10. A data processor formed on an LSI chip according to claim 9,

wherein the instruction cache memory stores the instruction address which is the physical address.

11. A data processor formed on an LSI chip comprising:

an instruction address generator;

an instruction cache memory;

an instruction decoder;

an operand address generator; and

an operand cache memory,

wherein the instruction address generator generates an instruction address,

wherein said instruction cache memory has entries each storing an instruction corresponding to the instruction address in its entry,

wherein into said instruction decoder is input an instruction from said instruction cache memory and said decoder outputs a decoded result,

wherein said operand address generator generates an operand address response to the decoded result of said instruction decoder,

wherein said operand cache memory has entries each storing operand data corresponding to the operand address in its entry,

wherein when the data processor executes a first instruction, the data processor invalidates the instruction and operand cache memories,

wherein the first instruction is stored in a main memory with other instructions, the main memory being external to the data processor,

wherein the instruction address generator generates the instruction address as a logic address, and

wherein an address of the main memory is a physical address.

12. A data processor formed on an LSI chip according to claim 11, further comprising:

an execution unit executing an instruction based on the decoded result at said instruction decoder,

wherein said instruction decoder and said execution unit can be operated in parallel.

13. A data processor formed on an LSI chip according to claim 12, further comprising:

a ROM storing a control information corresponding to an instruction,

wherein said ROM outputs the control information corresponding to an instruction output from said instruction cache memory.

14. A data processor formed on an LSI chip according to claim 12,

wherein each of entries in said instruction cache memory and said operand cache memory has a valid bit, and

wherein when said data processor executes the first instruction, the valid bits of said instruction cache memory and said operand cache memory are cleared.

15. A data processor formed on an LSI chip according to claim 12,

wherein each of said instruction cache memory and said operand cache memory is an associative memory.

16. A data processor formed on an LSI chip according to claim 11,

wherein each of said instruction cache memory and said operand cache memory is an associative memory.

17. A data processor formed on an LSI chip according to claim 11,

wherein each of entries in said instruction cache memory and said operand cache memory has a valid bit, and

wherein when said data processor executes the first instruction, the valid bits of said instruction cache memory and said operand cache memory are cleared.

18. A data processor formed on an LSI chip according to claim 11, further comprising:

a purge control unit;

wherein said purge control unit outputs the first instruction when the purge signal is input into said purge control circuit.

19. A data processor formed on an LSI chip according to claim 11, further comprising:

an address transformation circuit,

wherein into said address transformation circuit is input a logical address generated by said address generator and said address transformation circuit outputs a physical address corresponding to the logical address, and is connected to the output part inside of the LSI chip.

20. A data processor formed on an LSI chip according to claim 19,

wherein the instruction cache memory stores the instruction address which is the physical address.